

Connection and Calibration for LI152 v5

If the internal board layout is different to what is shown below then you need to use procedure CP15201.

Field Calibration

Apply power to module. With counter connected simulate zero input signal (example 4mA). By using "OFFS" trim potentiometer adjust for 0V±2mV on test socket below OFFS, (or TP1 internal). There should not be any pulse output over a longer period (zero lock out).

Apply full scale signal (example 20mA) and adjust "SPAN" for desired pulse output rate. It is recommended to use at least a 60 second interval to take pulse count.

Workshop Calibration / Re-Scaling

A complete re-scale requires housing removal. Separate the boards by removing screw in the centre. Select jumper positions on range selector from table, for desired maximum pulse output.

POS	P/MIN	Hz	Z		
			4020BC	4020BP	
			RS1= 62R	RS1 = 270R	
1	300-600	5-10	16	8	
2	150-300	2.5-5	32	16	
3	75.0-150	1.25-2.5	64	32	
4	37.5-75.0	0.6-1.2	128	64	
5	18.7-37.5	0.3-0.6	256	128	
6	9.3-18.7	0.16-0.30	512	256	
7	4.7-9.3	0.08-0.16	1024	512	
8	2.3-4.7	0.04-0.08	2048	1024	
9	1.2-2.3	0.02-0.04	4096	2048	
10	0.6-1.2	0.01-0.02	8192	4096	
11	0.3-0.6	0.005-0.01	16384	8192	



Calibration time can be shortened by calculating the frequency at test point 2.

The CD4020BC has outputs Q4 to Q14. The HEF4020BC has outputs Q3 to Q13.

As a result the frequency is different depending on what is fitted in IC2.

$$Hz(cal) = \frac{P/min}{60} \times Z$$
 (select Z from table above.)

Example: for 100p/min $Hz(cal) = \frac{100}{60} \times 64 = 106.66 Hz$

When the calibration frequency is established connect frequency counter to terminal 9 (common) and TP2 and adjust "SPAN" to this frequency. Verify correct calibration by measuring time interval of pulse output.

If zero requires re-calibration proceed as per 'FIELD CALIBRATION' procedure above. Internal zero point can be measured at TP1 on board.

Zero Lock Out

The LI152 is normally arranged for zero lock-out at 2% of input span (RL = 220k). For higher lock-out values change RL. For 5% lock out RL is equal to 150k.

To test lock-out connect voltmeter to pin 8 of IC1 and terminal 9 (0V). For signal >2% voltage should be approximately 12Vdc. For signal <2% voltage should be + 13Vdc.

Reverse Action

If a high pulse rate is required for a zero input signal **and** low pulse rate for full scale input **then** solder links need to be changed for reverse action.

Direct action: Solder links L2, L4 Reverse action: Solder links L1, L3

Note that "OFFS" now is used for full scale input and "SPAN" for zero input.

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APCS division	Drawing: CP15251 Issue: 3 9/12/21			Page: 1



Connection Examples



Note : Link from terminal 8 to 9 enables internal relay.

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